In the Claims:

Please cancel Claims 1-7, 10-16, 19-25, and 28-34 without prejudice. Applicant reserves the right to pursue the subject matter of Claims 1-7, 10-16, 19-25, and 28-34 in continuation applications.

1-7. (Canceled).

8. (Original) A transistor for an integrated circuit comprising:

a p-type substrate;

an n-type region disposed over said p-type substrate;

n-type buried layers disposed at about a boundary between said substrate and said n-type region, said buried layers doped to a higher level than said n-type region;

spaced apart p-type source and drain regions disposed in said n-type region forming a channel therein;

a control gate disposed above and insulated from said channel; and

said substrate, said n-type region and said n-type buried layers each biased such that said n-type region is fully depleted.

9. (Original) The transistor of claim 8 further including an isolation trench disposed in said n-type region and surrounding said source and drain regions, said isolation trench extending down into said substrate.

10-16. (Canceled).

17. (Original) A floating-gate transistor for an integrated circuit comprising:

a p-type substrate;

an n-type region disposed over said p-type substrate;

n-type buried layers disposed at about a boundary between said substrate and said n-type region, said buried layers doped to a higher level than said n-type region;

spaced apart p-type source and drain regions disposed in said n-type region forming a channel therein;

a floating gate disposed above and insulated from said channel;

a control gate disposed above and insulated from said floating gate; and

said substrate, said n-type region and said n-type buried layers each biased such that said n-type region is fully depleted.

18. (Previously Presented) The floating-gate transistor of claim 17 further including an isolation trench disposed in said n-type region and surrounding said source and drain regions, said isolation trench extending down into said substrate.

19-25. (Canceled).

26. (Original) A transistor for an integrated circuit comprising:

an n-type substrate;

a p-type region disposed over said n-type substrate;

p-type buried layers disposed at about a boundary between said substrate and said p-type region, said buried layers doped to a higher level than said p-type region;

spaced apart n-type source and drain regions disposed in said p-type region forming a channel therein;

a control gate disposed above and insulated from said channel; and

said substrate, said p-type region and said p-type buried layers each biased such that said p-type region is fully depleted.

27. (Original) The transistor of claim 26 further including an isolation trench disposed in said p-type region and surrounding said source and drain regions, said isolation trench extending down into said substrate.

28-34. (Canceled).

35. (Original) A floating-gate transistor for an integrated circuit comprising:

an n-type substrate;

a p-type region disposed over said n-type substrate;

p-type buried layers disposed at about a boundary between said substrate and said p-type region, said buried layers doped to a higher level than said p-type region;

spaced apart n-type source and drain regions disposed in said p-type region forming a channel therein;

a floating gate disposed above and insulated from said channel;

a control gate disposed above and insulated from said floating gate; and

said substrate, said p-type region and said p-type buried layers each biased such that said p-type region is fully depleted.

36. (Original) The floating-gate transistor of claim 35 further including an isolation trench disposed in said p-type region and surrounding said source and drain regions, said isolation trench extending down into said substrate.